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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
12/03/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/748,165	PAVER, NIGEL C.	
	Examiner	Art Unit	
	DAVID J. HUISMAN	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6-9,11-14,16 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-9,11-14,16 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/10/09 & 9/21/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-4, 6-9, 11-14, 16, and 23-25 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 6/10/2009, Amendment as received on 8/17/2009, and IDS as received on 9/21/2009.

Requirement for Information

3. The IDS filed on 6/10/2009 cites a decision and notification of reason(s) for refusal of patent by the JPO for a related application. In the notification of reason(s) for refusal, the JPO cited two documents deemed relevant to the application: Patent Publication Gazette No. 11-053189 and Patent Publication Gazette No. 2000-047998. Copies of these documents were not provided to the USPTO. Rule §1.105 states that *"In the course of examining or treating a matter in a pending or abandoned application filed under 35 U.S.C. 111 or 371…the examiner or other Office employee may require the submission, from individuals identified under §1.56(c), or any assignee, of such information as may be reasonably necessary to properly examine or treat the matter, for example:…(iii) Related information: A copy of any non-patent literature, published application, or patent (U.S. or foreign), by any of the inventors, that relates to the claimed invention."* Per this rule, the examiner requires that applicant cite and submit translated copies of the aforementioned documents cited by the JPO so that they may be considered.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The disclosure is again objected to because of the following informalities:

- On page 8, line 1, please correct the phrase "Fig.3 is an of an example…".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3-4, 6-9, 11-14, 16, and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Golston, U.S. Patent No. 6,026,484.

8. Referring to claim 1, Golston has taught a device comprising:

a) a status register to store a word including a plurality of arithmetic flags, each flag associated with one of a plurality of data items of varying field sizes and wherein the word is a single instruction multiple data (SIMD) word. See Fig.5, status register 211, column 13, lines 3-5, and column 21, line 56, to column 22, line 17.

b) a combination function module to logically combine the plurality of arithmetic flags within the word into a single combined arithmetic flag variable, and to store the single combined arithmetic flag variable into a second register (see Fig.5, register 210, and column 19, lines 1-

46), wherein in combining, the combination function module performs an OR operation (see column 19, lines 14-22).

c) wherein each of the plurality of arithmetic flags represents a result status of the plurality of a mathematical operation performed by a processor to obtain one of the plurality of data items. Essentially, multiple arithmetic operations may be performed at once to produce multiple result data items. For instance, if there are four parallel operations, then four arithmetic flags will be set in register 211 (Fig.5). Then, the arithmetic flags are combined into one flag (via OR operation) and the combined result is stored in the appropriate flag section of register 210 (Fig.5 and Fig.6).

d) a condition check module to determine the result status of the combined arithmetic flag variable and cause the processor to execute an appropriate operation based on the result status. See column 5, lines 39-40. Note that the status bits are checked to control conditional execution, as is known in the art.

e) Golston has not taught storing, in the status register, a word including a plurality of sets of arithmetic flags, each set having M bits, wherein the status register can store sets of varying field size, and that the combination function module examines the word stored in the status register to determine a data item field size of each set of arithmetic flags for the word (see Table 4 in column 22, and note that size must be determined to determine which bits to combine), and based on the determination of the data item field size, to perform the logical combining of the plurality of arithmetic flags of the sets within the word into a single combined arithmetic flag variable of M bits. That is, Golston has taught storing just a single flag bit at a time for each data item and combining each data item's flag bit into a single combined arithmetic variable

comprising a single bit. See column 21, lines 41-45, Table 4 in column 22, and the examples in columns 77-78. For instance, in Table 4, Golston shows storing four carry bits for four 8-bit data items, and then combining those four carry bits into a single, global carry bit (column 19, lines 17-22). Similarly, two carry bits for two 16-bit data items would be combined into a single, global carry bit. However, Golston has also taught the general concept of storing multiple status flags in a single register, as is known in the art (see Fig.6, and note that negative (N), carry (C), overflow (V), and zero (Z) bits are generally stored in the same register). In addition, Golston has taught that it is desirable to also store and combine all of the arithmetic flags. See column 19, lines 1-46, column 21, lines 41-45, and column 22, lines 14-17. As a result, in order to indicate more than one status for each data item at a given time, as currently proposed by Golston, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Golston to store multiple status indications for each data item, and multiple global status indications would be realized after combining the sets of flags. This could be done by increasing the size of the flags register so that more flags may be stored. One that would be willing to trade more hardware for increased status indication functionality would be motivated to make such a modification given that it is already known to store all arithmetic flags at once on a smaller scale (as shown in Fig.6). Or, one of ordinary skill in the art would have recognized that the flags register is 32 bits wide and that the carry bits require at most 4 of those bits (the rest are filled with zeros). Hence, one could use some of those zero bits to store bits for N, V, and Z flags. Either way, storing more flag data would allow the system to branch based on different statuses. Note further that the set size is inherently determined because the system must know how many flags to combine, and there are different numbers of flags based on the data

size. For instance, if the set size is 8, then four of each type of flag must be combined. On the other hand, if the set size is 16, then two of each type of flag must be combined. See Table 4 in column 22.

9. Referring to claim 3, Golston, as modified, has taught the device recited in claim 1, wherein the field size is based on a nibble, byte, half-word, or word in length. See column 20, Table 2, and lines 38-45).

10. Referring to claim 4, Golston, as modified, has taught the device recited in claim 3, wherein the plurality of arithmetic flags further comprise a negative data value, a zero data value, a carry out occurrence in a data value, or an overflow condition in a data item in the plurality of data items. See Fig.6 and column 19, lines 1-46.

11. Referring to claim 6, Golston, as modified, has taught the device recited in claim 1, wherein the result status determined by the condition further comprises:

a) any data item has overflowed. See column 19, lines 23-37, and note that if the V bit set, overflow is detected.

b) any data item has not overflowed. See column 19, lines 23-37, and note that if the V bit is clear, overflow is not detected.

c) any data item is positive or zero. See column 19, lines 1-13, and note that if the N bit is clear, a positive or zero data item is detected.

d) any data item is negative. See column 19, lines 1-13, and note that if the N bit is set, a positive or zero data item is detected.

e) any data item is zero. See column 19, lines 38-46, and note that if the Z bit is set, a zero data item is detected.

f) any data item is not zero. See column 19, lines 38-46, and note that if the Z bit is clear, a zero data item is detected.

g) any data item has a carry out. See column 19, lines 14-22, and note that if the C bit is set, a carry is detected.

h) any data item does not have a carry out. See column 19, lines 14-22, and note that if the C bit is clear, a carry is not detected.

i) all data items have overflowed. See column 19, lines 23-37, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so overflow of all data items can be checked.

j) all data items have not overflowed. See column 19, lines 23-37, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so non-overflow of all data items can be checked.

k) all data items are positive or zero. See column 19, lines 1-13, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so all data items can be checked to see if they are zero or positive.

l) all data items are negative. See column 19, lines 1-13, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so negativity of all data items can be checked.

m) all data items are zero. See column 19, lines 38-46, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so all data items can be checked to see if they are zero.

n) all data items are not zero. See column 19, lines 38-46, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so all data items can be checked to see if they are non-zero.

o) all data items have a carry out. See column 19, lines 14-22, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so carry out of all data items can be checked.

p) all data items do not have a carry out. See column 19, lines 14-22, and column 20, lines 46-50. Note that a flag is set/cleared for each data item so non-carry out of all data items can be checked.

12. Referring to claim 7, the method of claim 7 is performed by the device of claim 1. Consequently, claim 7 is rejected for the same reasons set forth in the rejection of claim 1.

13. Referring to claim 8, Golston, as modified, has taught a method as described in claim 7. Furthermore, claim 8 is rejected for the same reasons set forth in the rejection of claim 3.

14. Referring to claim 9, Golston, as modified, has taught a method as described in claim 8. Furthermore, claim 9 is rejected for the same reasons set forth in the rejection of claim 4.

15. Referring to claim 11, Golston, as modified, has taught a method as described in claim 7. Furthermore, claim 11 is rejected for the same reasons set forth in the rejection of claim 6.

16. Referring to claim 12, claim 12 is rejected for the same reasons set forth in the rejection of claim 7.

17. Referring to claim 13, Golston, as modified, has taught an apparatus as described in claim 12. Furthermore, claim 13 is rejected for the same reasons set forth in the rejection of claim 3.

18. Referring to claim 14, Golston, as modified, has taught an apparatus as described in claim 13. Furthermore, claim 14 is rejected for the same reasons set forth in the rejection of claim 4.

19. Referring to claim 16, Golston, as modified, has taught an apparatus as described in claim 12. Furthermore, claim 16 is rejected for the same reasons set forth in the rejection of claim 6.

20. Referring to claim 23, claim 23 is rejected for the same reasons set forth in the rejection of claim 1.

21. Referring to claim 24, Golston, as modified, has taught the system of claim 23, wherein the processor includes at least three stages of pipelining. See Fig.4.

22. Referring to claim 25, Golston, as modified, has taught the system of claim 24, wherein the at least three stages of pipelining include a fetch stage, a decode stage, and an execute stage. See Fig.4, and note the fetch and execute stages. In between is a decode stage, which accepts fetched instructions, decodes them, and sends the execution unit the appropriate signals. See Fig.5, component 250.

Response to Arguments

23. Applicant's arguments filed on August 17, 2009, have been fully considered but they are not persuasive.

24. Applicant argues the novelty/rejection of claim 1 on pages 8-9 of the remarks, in substance that:

> (1) "Claim 1 recites the presence of a status register that stores multiple sets of arithmetic flags, where each set is associated with one of multiple data items, and further that after a logical combination of the flags of the sets, a single combined arithmetic flag variable is stored into a second register. The art including Golston fails to teach or suggest this status register. In this regard, neither register 210 nor register 211 of Golston can be the recited status register of the claim. That is, neither register 210 nor register 211 can store multiple sets of arithmetic flags. Clearly as seen, register 210 simply stores a single set of flags. In turn, multiple flags register 211 can, based on a given operation of the Golston system, only store a single type of flag, although it may store multiple of this flag for different data elements. Golston, column 21, lines 41-45. This can be further seen in the various details of different operations performed in Golston, such as described with regard to the examples in columns 77-78 of Golston. As seen, only a single flag type is stored at a given time within multiple flags register 211.
>
> Nor would it be obvious for the system of Golston to be modified to provide a status register having multiple sets of flags. Instead it appears that Golston is concerned with only a given type of flag for any given operation (e.g., column 21). In contrast, the recited a subject matter describes that each set includes multiple arithmetic flags for each data item obtained by performance of a mathematical operation.

> (2) Furthermore, nothing in Golston anywhere teaches or suggests that a determination is made as to any data item field size for each set of arithmetic flags. Instead, as discussed above Golston is concerned with only a single flag at a time. Furthermore, the determination contended by the Office Action with regard to Table 4 simply shows that a single type of flag can be stored in a given bit position. Nonetheless, nothing in the reference anywhere teaches or suggests that a combination function module examine this word itself to determine a data item field size for the sets of flags. Instead, all that is taught is that a field size of a status register indicates the data size of multiple operations that are to be performed. Golston, col. 20, lns. 33-35. However, there is no determination of a size of sets of flags, particularly as Golston fails to teach the presence of such sets, and further as the status register 210 includes only one, fixed field size set of flags."

25. These arguments are not found persuasive for the following reasons:

a) Regarding the first argument, the examiner asserts that applicant is correct in pointing out that Goltson only explicitly shows storing one type of flag (carry). However, the examiner had stated in the rejection that it would have been obvious to store multiple sets of multiple flags. While Golston just shows storing a carry flag for each data item, it is known to store carry, zero, negative, and overflow flags for each data item. Such flags are even disclosed in Golston (column 19, lines 1-46). The simultaneous storing of each flag is simply not shown. However, condition/status/flag registers are known to store all flags together. Hence, it would have been obvious to store each type of flag for each data item so that the execution of subsequent operations may be conditional on different statuses. One could either increase the size of the status register or replace some of the zeros with actual flag bits (Table 4 in column 22).

b) Regarding the second argument, Golston inherently determines the size of the data item field size. This is performed because the size indicates the number of flags to combine into a global flag. If the data items are 8-bits, then there are four flags to combine for each status (four carries, four negatives, four zeros, and four overflows). However, if the data items are 16 bits, then there are only two flags to combine for each status (two carries, two negatives, two zeros, and two overflows). Thus, the system must determine the field size to also determine how many flags must be combined to generate the global flags.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183